High-Impedance Bus Differential Misoperation Due to Circuit Breaker Restrikes

Kristian Koellner
Lower Colorado River Authority

Oskar Reynisson and David Costello
Schweitzer Engineering Laboratories, Inc.

This paper was presented at the 67th Annual Conference for Protective Relay Engineers and can be accessed at: http://dx.doi.org/10.1109/CPRE.2014.6799013.

For the complete history of this paper, refer to the next page.

Presented at the
67th Annual Conference for Protective Relay Engineers
College Station, Texas
March 31–April 3, 2014

Previously presented at the
40th Annual Western Protective Relay Conference, October 2013

Previous revised editions released December 2013, August 2013, and May 2013

Originally presented at the
67th Annual Georgia Tech Protective Relaying Conference, May 2013

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Kristian Koellner, *Lower Colorado River Authority*
Oskar Reynisson and David Costello, *Schweitzer Engineering Laboratories, Inc.*

***Abstract*—This paper discusses the potential misoperation of a high-impedance bus differential relay when surge arresters are located within the relay zone of protection. Transient overvoltage caused by a circuit breaker restrike during shunt capacitor bank de-energization can cause the surge arresters to conduct. The relay interprets the current flowing through the surge arrester as fault current within its zone of protection and subsequently trips the bus.**

This paper reviews high-impedance bus differential protection principles and discusses circuit breaker design, voltage rating, and restrikes. Trapped charge on shunt capacitor banks is analyzed, and surge arrester design and operation are reviewed. This paper also analyzes real-world events that show relay misoperation due to circuit breaker restrikes and are validated by computer restrike simulations. This paper shows that a better understanding of transient overvoltages is essential to improving protection settings in order to minimize false trips while maintaining fast, secure, and sensitive bus protection.

I. Introduction

Shunt capacitor banks are added to substation buses for voltage and reactive power support. When a capacitor bank is de-energized, a trapped charge remains on the capacitor. The amount of trapped charge depends on the moment of de-energization relative to the voltage and current waveforms (i.e., when the breaker actually interrupts the capacitor bank current flow). A large amount of trapped charge on the capacitor bank results in an increased voltage across the open circuit breaker. If the voltage across the circuit breaker exceeds the dielectric strength of the circuit breaker, the circuit breaker can restrike. A restrike results in a transient overvoltage at the bus that can cause nearby surge arresters to conduct. When a surge arrester is included in a bus zone, any time that the surge arrester conducts current, that current results in a differential current in the protected zone because no current transformer (CT) monitors the current through the surge arrester. This differential current is identical to that for a fault inside the bus zone, so a protective device cannot distinguish between these two types of current. High-impedance bus protection is usually set sensitive. If a surge arrester is within the zone of protection, it must be taken into consideration when relay settings are determined because of the fast operating time of the high-impedance bus protection.

This paper presents a detailed Electromagnetic Transients Program/Alternative Transients Program (EMTP/ATP) model of a 138 kV substation that includes circuit breakers, surge arresters, buswork, and capacitor banks. The model is used to simulate the transient behavior of the bus voltage during a capacitor bank de-energization followed by a circuit breaker restrike. The EMTP/ATP model is used to validate a real-world high-impedance bus differential relay misoperation during capacitor bank de-energization.

II. Shunt Capacitor Banks

Shunt capacitor banks are installed in the power system at nearly all voltage levels to provide local voltage and reactive power (VAR) support. Generating reactive power locally minimizes the need to transfer reactive power across the power system [1] [2]; therefore, the transfer capacity of transmission and distribution lines can be reserved for the transfer of real power that cannot be generated locally. Fig. 1 shows a grounded-wye, 31.2 MVAR shunt capacitor bank installed at a 138 kV substation.

Fig. 1. 31.2 MVAR shunt capacitor bank at 138 kV substation.

Capacitor bank switching causes transient-related issues at the substations where shunt capacitor banks are installed. These issues are proportional to the system voltage level and the system X/R ratio. Energization of shunt capacitor banks causes inrush currents with high magnitude and frequency.

An equivalent diagram of the substation under study is shown in Fig. 2.

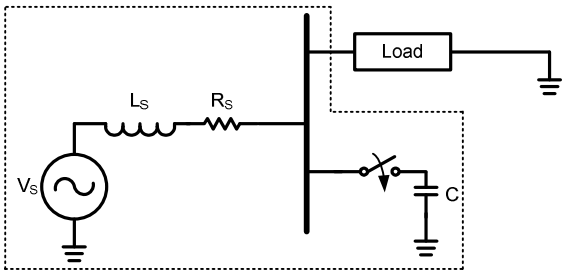

Fig. 2. Shunt capacitor bank energization equivalent diagram.

In Fig. 2, the variables are defined as follows:

- V_S is the source voltage.
- L_S is the source inductance.
- R_S is the source resistance.
- *C* is the capacitance of the shunt capacitor.

Neglecting the load and assuming that the source resistance is very small, the system shown in Fig. 2 becomes a simple series LC circuit. Assuming this simple series LC circuit, the capacitor bank energization inrush current can be calculated using (1).

$$i(t) = \frac{V(0)}{Z_0}\sin(\omega_0 t) \qquad (1)$$

where:

V(0) = the difference between the source voltage and the initial voltage of the capacitor at the moment of energization.

$$Z_0 = \sqrt{\frac{L_S}{C}}$$

$$\omega_0 = \frac{1}{\sqrt{L_S C}}$$ (the resonance frequency)

Equation (1) shows that the magnitude of the energization inrush current depends on the voltage level at the moment of energization and the characteristic impedance of the LC circuit. Fig. 3 shows a typical worst-case inrush current for a shunt capacitor bank energization. The high-frequency inrush current only lasts for approximately 20 milliseconds.

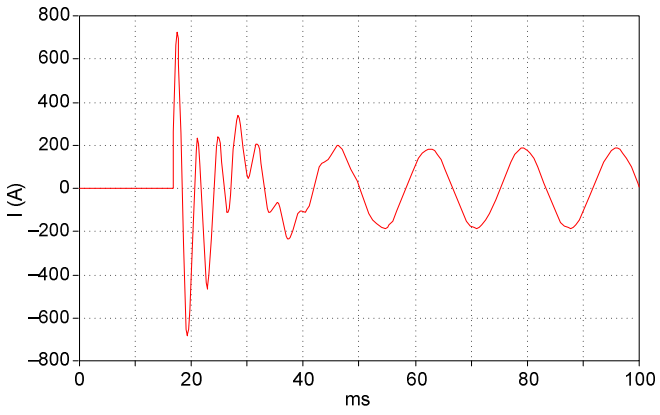

Fig. 3. Shunt capacitor bank energization inrush current.

As the inductance increases, both the peak current and its frequency decrease. On the other hand, as the capacitance increases, the peak current increases and its frequency decreases. The most common method of limiting the peak inrush current is to add inductance or resistance to the LC circuit. Adding inductance or resistance to the LC circuit is done either by installing a current limiting reactor in series with the capacitor or by installing a temporary preinsertion resistor in the circuit breaker connecting the capacitor to the bus. The current limiting reactor is always a part of the circuit, but the resistor is only a part of the circuit during breaker open/close operations. The resistor is bypassed once the capacitor bank is energized or de-energized [3]. The substation under study uses preinsertion resistors to limit the capacitor bank inrush currents.

Shunt capacitor bank de-energization is highly demanding on the dielectric performance of the circuit breaker [4]. During the de-energization of a capacitor bank, the circuit breaker is stressed by a transient recovery voltage (TRV) that can be as high as twice the peak system voltage. TRV for high-voltage circuit breakers is the voltage that appears across the circuit breaker terminals after current interruption. TRV may cause dielectric breakdown and the reestablishment of current flow through the circuit breaker. The reestablishment of current flow through the circuit breaker is called a restrike when the reestablishment of current occurs 0.25 cycles after the initial current interruption [5].

When a capacitor bank is de-energized, the charge on the capacitor (q = CV) at the moment of de-energization is trapped in the capacitor, as shown in Fig. 4.

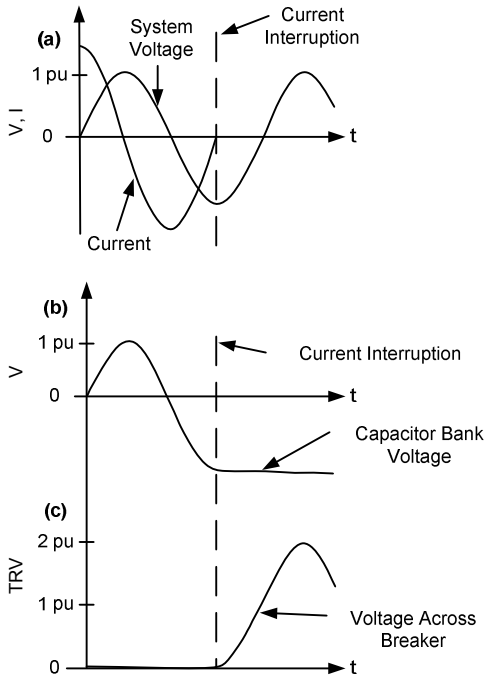

Fig. 4. Capacitor voltage and current.

Fig. 4a shows the system voltage and the current flowing through the capacitor bank circuit breaker at the moment of capacitor bank de-energization. Because the load is purely capacitive, the current leads the voltage by 0.25 cycles, or

90 degrees. The circuit breaker interrupts the current at or very close to the current zero crossing, when the voltage is at its maximum. Voltage maximum means that the capacitor is charged to the maximum value and the charge at the moment of de-energization is trapped in the capacitor. The trapped charge holds the capacitor voltage at its maximum value (see Fig. 4b). Fig. 4c shows the TRV across the circuit breaker. The capacitor voltage stays at its maximum value due to the trapped charge. One-half cycle after the circuit breaker opens, the system voltage is at the opposite maximum value, resulting in twice the peak voltage appearing across the capacitor bank circuit breaker.

IEEE Standard 18-2002 states that trapped charge on a capacitor bank must dissipate so that 5 minutes after capacitor bank de-energization, the voltage across the capacitor is not more than 50 V [2]. For the purpose of this transient capacitor bank study, it is assumed that the capacitor voltage is constant immediately after the circuit breaker opens.

The current flowing through a circuit breaker is normally not interrupted when the circuit breaker contacts begin to separate. When the circuit breaker contacts separate, the current continues to flow through an arc until the current reaches the next zero crossing. The high current creates metal vapor, and this metal vapor creates a conductive path that allows the current to continue flowing. The metal vapor requires a high temperature. When the current approaches the zero crossing, the current flow can no longer support the heat needed to maintain the arc, so the arc suddenly decreases or "chops out" [6]. Current chop means that the current is not interrupted exactly at the zero crossing. Modern SF6 circuit breakers have a low current chop value of approximately 3 to 5 A, which minimizes the current chop [7]. The substation under study is equipped with SF6 circuit breakers.

Circuit breaker current interruption is a process that takes approximately 3 to 5 power system cycles [8]. Interruption time is defined as the time it takes the circuit breaker contacts to fully separate. However, the current must be interrupted before the contacts are fully separated. The dielectric strength, or insulation, of the gap between the opening circuit breaker contacts increases as the contacts move farther apart (the gap widens). The dielectric strength of the gap of an opening circuit breaker as a function of time is shown by Curves A and B in Fig. 5.

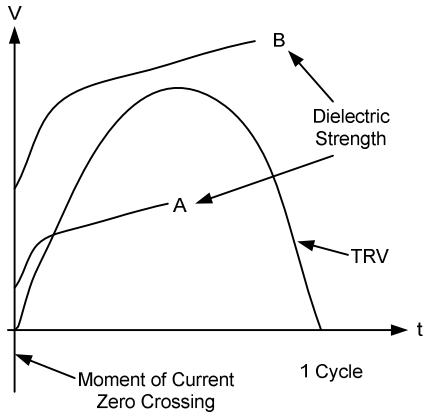

Fig. 5. TRV and dielectric strength across circuit breaker.

Curves A and B show the rise of dielectric strength recovery across the circuit breaker immediately after the initial current interruption. The curve depends on when the circuit breaker contacts begin to separate, with respect to the current wave. Curve A, which shows low interruption effectiveness, happens when the circuit breaker contacts begin to separate right before the current zero crossing. Curve B shows higher interruption effectiveness. The circuit breaker contacts begin to separate soon enough that the gap has enough dielectric strength to prevent a restrike when the voltage across the circuit breaker reaches 2 pu. The initial slope of the dielectric recovery may be fairly steep, but the curve tends to level off at the breakdown strength of the maximum contact gap [9].

Fig. 6 shows capacitor bank de-energization followed by a circuit breaker restrike. The current is interrupted at the zero crossing, and at that instant, the system voltage and the capacitor voltage are at negative maximum value. The capacitor voltage stays at the negative maximum value due to the trapped charge left on the capacitor. One-half cycle after the interruption, the system voltage reaches its positive maximum value, resulting in twice the maximum voltage value appearing across the circuit breaker. The high-voltage potential across the contacts may exceed the dielectric strength of the gap at that moment. The breakdown of the dielectric strength results in an arc that reestablishes current flow (i.e., a restrike). Restrike current is the same as energization inrush current that can be calculated using (1) but with a 2 pu voltage difference between the bus and the capacitor. The 2 pu voltage difference results in restrike currents having twice the magnitude of the worst-case inrush current, where the voltage difference is only 1 pu. The restrike current has a much higher frequency than the power system current, as shown for inrush currents by (1). At the next restrike current zero crossing, the current is interrupted again. By this time, the circuit breaker contacts are farther apart, making a second restrike much less likely [9] [10].

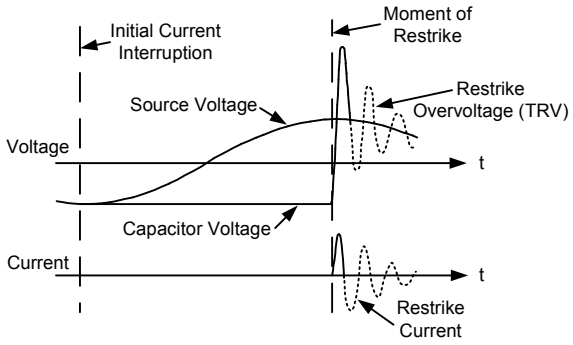

Fig. 6. Voltages and current circuit breaker restrike.

III. Surge Arresters

The substation under study is equipped with metal oxide surge arresters. The surge arresters are installed throughout the power system to protect power system equipment from transient overvoltages. Power system equipment is generally not designed to withstand lightning and switching overvoltages. Power system equipment vulnerable to

overvoltages includes power transformers, instrument transformers, and circuit breakers.

Fig. 7 shows how surge arresters limit the overvoltage to voltage levels within the equipment voltage rating. Surge arresters are installed on the power system in overvoltage coordination fashion. The surge arresters must act before the overvoltage exceeds the equipment rating.

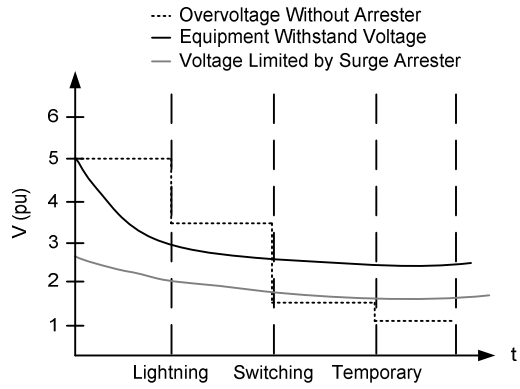

Fig. 7. Overvoltage duration, effects of surge arresters, and equipment rating.

Surge arresters increase the equipment service life because equipment exposure to excessive overvoltages can lead to insulation breakdown, which causes premature equipment failure.

The surge arrester is a varistor that has extremely nonlinear voltage versus current characteristics. Modern metal oxide surge arresters contain ceramic varistors that are either made from zinc oxide (ZnO) or bismuth oxide [11]. To effectively protect the power system equipment, the surge arrester has to fulfill the following two design requirements [12]:

- Provide overvoltage protection for the system, which means that the surge arrester has to limit the voltage to within the voltage range of the equipment, with some safety margin.
- Be thermally stable during the most severe operating conditions, which means that the surge arrester must dissipate the extra energy caused by the overvoltage conditions. Thermal stability means that the internal temperature cannot exceed some specific value under both normal and fault conditions and under both normal voltage and maximum operating voltage conditions. If the internal temperature exceeds the specific value, the heat cannot be dissipated effectively and the arrester can become thermally unstable (the arrester heats up) and might be destroyed.

The surge arresters at the substation under study are 84 kV metal oxide varistor (MOV) surge arresters. They are mounted on the bus with one surge arrester per phase. The discharge characteristics are shown in Fig. 8.

Fig. 8 shows the peak phase voltage, V (kV), as a function of conducted current, I (kA). The bus under study is rated 138 kV (phase-to-phase root-mean-square [rms] voltage), which results in 113 kV peak phase-to-ground voltages. Fig. 8 shows that the surge arrester starts conducting when the phase voltage exceeds approximately 200 kV (1.75 pu of system voltage).

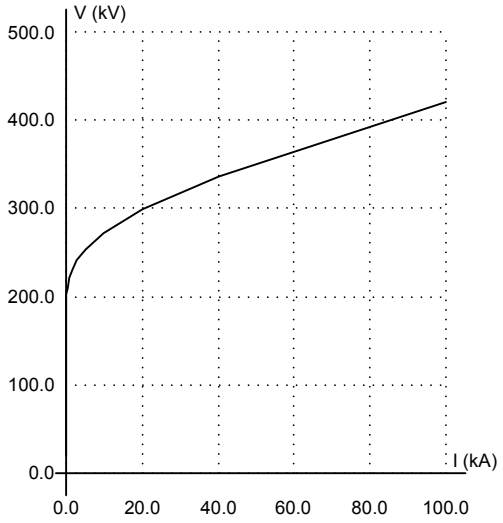

Fig. 8. Surge arrester V-I characteristics.

Fig. 9 shows that the surge arrester starts conducting when the system voltage exceeds approximately 1.75 pu of nominal voltage. The surge arrester conducts for every other half cycle of the restrike current. The restrike current has the same frequency as the energization inrush current, which is the same frequency as the resonance frequency of the LC circuit shown in Fig. 2 (approximately 400 to 600 Hz). This frequency is much higher than the nominal frequency of the power system [13].

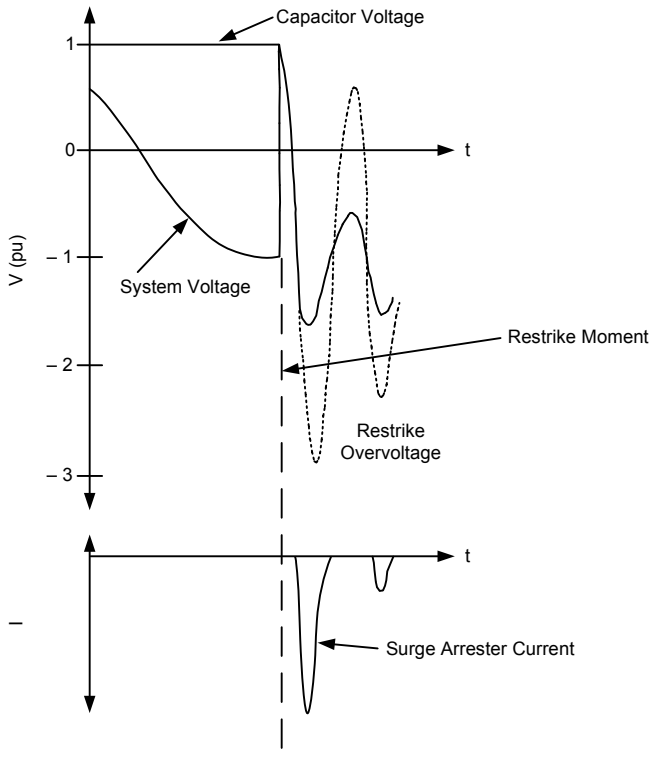

Fig. 9. System voltage and surge arrester current during a circuit breaker restrike.

IV. High-Impedance Bus Differential Protection

Kirchhoff's current law states that the vector sum of all currents entering and leaving a node or bus is equal to zero. Kirchhoff's current law is the basic principle behind bus differential protection used in power systems. A bus differential scheme simply adds together the currents entering and leaving the bus, as shown in Fig. 10. A difference between all the currents above some predefined threshold is an indication of a bus fault, and therefore, the bus must be de-energized quickly.

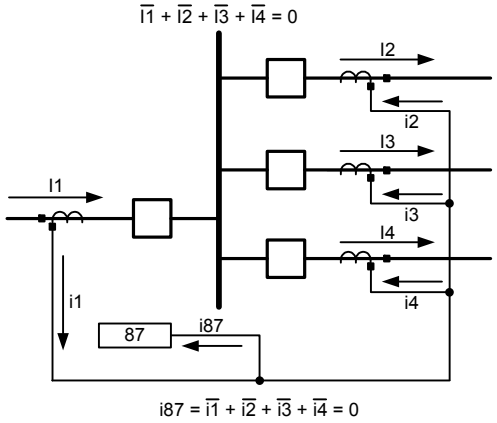

Fig. 10. Basic bus differential protection.

A simple current differential scheme can be implemented by paralleling the CTs from all the circuit breakers on the bus. In this case, the sum of the currents for each phase should be zero for normal through-load and external fault conditions. The first complication with this scheme is that it requires all of the paralleled CTs to have the same CT ratio (CTR) to ensure that all the secondary currents are compared on the same basis as the primary currents. The relay for this scheme measures the difference in currents (i.e., the differential element [ANSI 87] that can be set with very sensitive pickup because, ideally, no current should flow to the relay under normal load or external fault conditions). Another requirement imposed by this scheme, especially if the pickup is set to be very sensitive, is that all CTs must behave the same way under all possible operating conditions, including external faults with heavy fault current and asymmetrical offset caused by high system X/R ratios [14]. The purpose of this paper is not to describe the operation of the high-impedance bus differential relay in detail (for more details, refer to [15]).

Conventional iron-core CTs can saturate, regardless of their ratio and accuracy class. Saturation causes the CT secondary output current to not represent the primary current flowing on the power system. Poor CT behavior causes a difference in secondary currents that results in differential current flowing to the relay. The relay cannot distinguish differential current due to an internal bus fault from CT saturation during an external fault [14] [15].

High-impedance bus differential relays are applied to the parallel output of all CTs from each phase connected to a common bus. As mentioned previously, all the paralleled CTs must have the same ratio and proper polarity to ensure that the secondary outputs add up to zero (i.e., cancel each other out).

Any difference in current has to flow through the relay, which has a large resistor in series with the relay. The large resistor causes a high-voltage drop across the relay. The high-impedance differential relay is set to trip if the voltage rises above a predefined threshold. The high-impedance differential relay is extremely sensitive to the detection of bus faults; therefore, the CTs must have the same ratio and be of the same accuracy class to minimize differential currents related to CT performance.

For through-fault conditions, it is most likely that the faulted feeder CT will saturate because it is carrying the most current. The high-impedance bus differential relay voltage threshold must be set above the voltage created by one CT being completely saturated, because a completely saturated CT does not produce any secondary current. The equivalent circuits for both normal load conditions and external fault conditions are shown in Fig. 11 and Fig. 12.

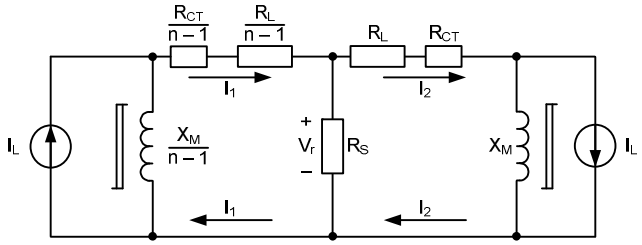

Fig. 11. High-impedance bus differential equivalent circuit for normal operating conditions.

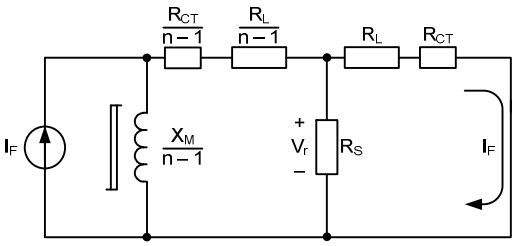

Fig. 12. High-impedance bus differential equivalent circuit for external fault conditions.

For an external fault with a saturated CT, Fig. 12 shows how the saturated CT creates a current path through its secondary CT resistance R_{CT}, but it does not have any secondary current contribution. The CT lead and internal resistance are very small compared with the internal resistance of the relay R_S; therefore, the worst-case voltage V_r across the relay is equal to the voltage drop across the CT lead and internal resistance under maximum external fault conditions. The relay voltage threshold must be set above the highest voltage developed across the high-impedance element. Usually, the voltage V_r is multiplied by a safety factor of at least 1.5 for worst-case external faults.

The voltage drop that must be calculated for each circuit or feeder connected to the bus is shown in (2).

$$V_r = \frac{I_F}{N} \bullet (R_{CT} + R_L \bullet k) \quad (2)$$

where:

I_F = the maximum fault current.

N = the CTR (tapped CTR).

R_{CT} = the CT secondary winding and lead resistance up to the CT terminals.

R_L = the one-way resistance of a lead from the junction points to the most distant CT.

k = 1 for three-phase faults and 2 for single-phase-to-ground faults.

The pickup setting for the relay should be set using (3).

$$V_s = K \bullet V_r \quad (3)$$

where:

K = a safety factor to ensure secure operation.

This calculation is accurate as long as the CT leads are routed individually to a common junction point. The safety factor is normally set to 1.5 or higher.

V. Misoperation Due to Circuit Breaker Restrike

The substation under study is a 138 kV substation that has two incoming lines, two outgoing feeders serving generic load through step-down transformers, a capacitor bank, and a surge arrester. The one-line diagram for the substation is shown in Fig. 13. The substation bus is protected using a high-impedance bus differential scheme. All the CTs are the same accuracy class, and all five CT secondary circuits are paralleled to the high-impedance relay.

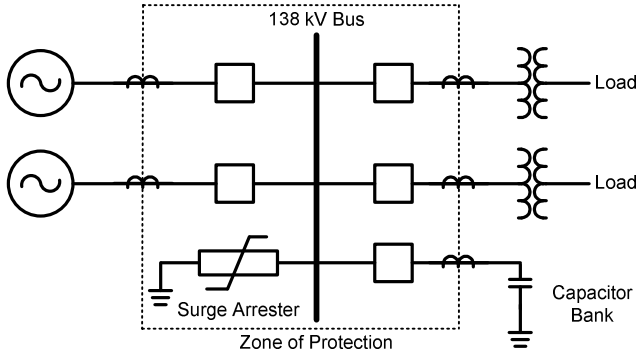

Fig. 13. 138 kV substation under study.

Additional information about the system is as follows:

- The shunt capacitor bank is fused-style, solidly grounded 31.2 MVAR.
- The shunt capacitor bank circuit breaker is a 2000 A, 40 kA SF6 circuit breaker.
- The line CTs are 1200:5, and the capacitor bank CT is 2000:5 tapped at 1200:5. They are all C800 rated.
- The surge arrester is rated for 84 kV. The characteristics are shown in Fig. 8.

The high-impedance bus differential relay at the substation was set to 75 V with no additional time delay, based on (2) and (3).

The capacitor bank is energized and/or de-energized manually by system operators as needed. Following one such de-energization, the high-impedance bus protection detected a differential current on C-phase and tripped the 138 kV bus. There was no evidence of a bus fault at the substation, and there were also no fault indicators at adjacent substations (i.e., no Zone 2, Zone 3, or ground overcurrent elements picked up).

Fig. 14 shows the event report created by the high-impedance bus differential relay immediately after the capacitor bank de-energization. The event report shows the voltage measured by the differential element that operated during the event. The event report shows a spike in the C-phase voltage before the C-phase differential element (87C1) asserts and trips the relay.

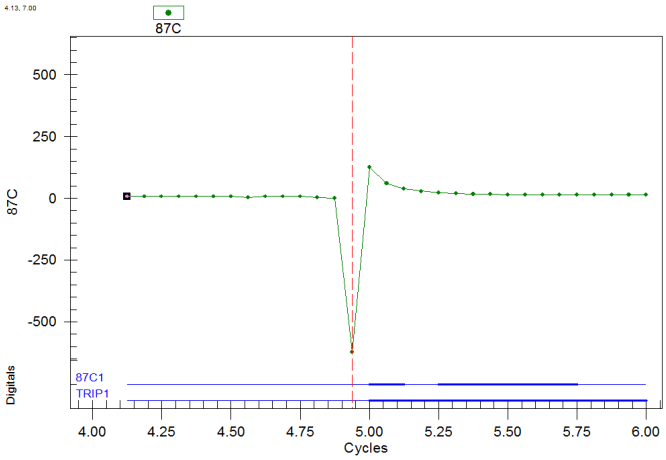

Fig. 14. Event report showing differential current and relay elements.

Fig. 14 shows 2 cycles before and after the event. The relay samples the currents 16 times per power system cycle, and the protection logic is processed 8 times per power system cycle. Fig. 14 shows that the spike consists of only one sample point, and then, 0.0625 cycles later, the relay trips.

Fig. 14 is a raw relay event report. Raw event reports show exactly what the relay is sampling. However, the sampled signal may not exactly represent the current flowing on the power system. The power system currents are first measured by CTs and then passed through an analog low-pass filter before the relay samples the currents.

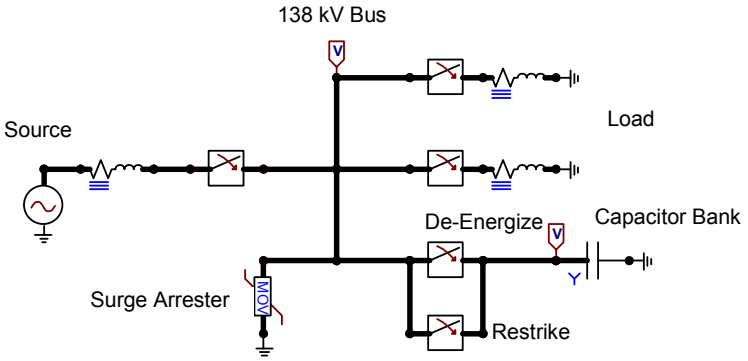

Fig. 15. Model of the 138 kV substation.

As previously stated, there was no evidence of faults at adjacent substations and there were no signs of short circuits at the substation bus itself. Therefore, the relay misoperation was suspected to be related to the capacitor bank de-energization. Based on the substation and event information, a likely theory of what happened is as follows:

- The capacitor bank was de-energized.
- The trapped charge maintained high voltage on the capacitor.
- There was a capacitor bank circuit breaker restrike creating a transient overvoltage at the substation bus.
- The surge arrester located at the bus started conducting current due to the high transient overvoltage.
- The surge arrester current appeared to the high-impedance bus differential relay as differential current.
- The relay tripped on the differential current and de-energized the bus.

To simulate capacitor bank de-energization followed by a circuit breaker restrike, an EMTP/ATP model of the substation was created [13] [16]. This model is shown in Fig. 15.

Some additional details of this model are as follows:

- The source is a 138 kV Thévenin voltage source providing rated short-circuit currents at the bus.
- The two step-down transformers are neglected because the nonlinear characteristics of the transformer are not important for this study.
- The downstream load is modeled as an RL branch.
- The capacitor bank is modeled as grounded, wye-connected capacitance.
- The surge arrester is modeled as “MOV - exponential current-dependent resistor, TYPE 92” [16], using the nonlinear characteristics shown in Fig. 8.

A capacitor bank de-energization followed by a circuit breaker restrike 0.5 cycles later was simulated, and the differential current (the current through the surge arrester) for C-phase is shown in Fig. 16. To provide a better comparison with what the relay is measuring, the current was passed through an analog low-pass filter. The analog low-pass filter caused a decrease in current magnitude and a shift in the phase.

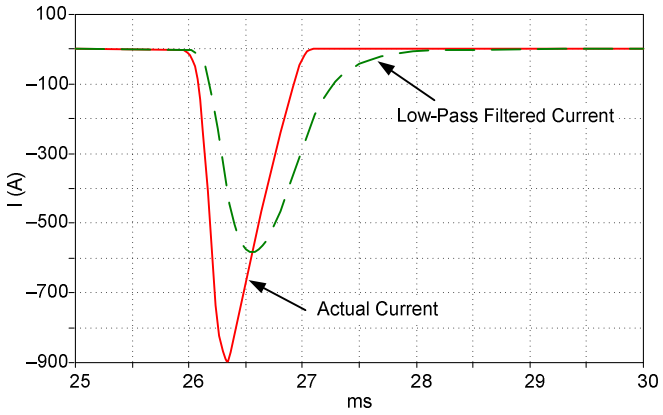

Fig. 16. Simulated current spike—actual current and low-pass filtered current.

A comparison of Fig. 14 and Fig. 16 shows that the current in Fig. 16 has a very similar shape to the voltage shown in Fig. 14. Note that Fig. 14 shows secondary voltage (secondary current multiplied by 2,000 Ω) and Fig. 16 shows primary current.

The main difference between the simulated current waveform in Fig. 16 and the actual voltage waveform measured by the relay in Fig. 14 is that the simulated maximum only has a negative value, but the actual event has a large negative spike and then bounces to a positive voltage value before decaying to zero. The positive values are caused by the nonlinear excitation branches of the CTs, which the

model does not take into account. When a primary fault current is interrupted, the CT secondary output does not immediately follow the primary current to zero, especially when the current has severe dc offset. The trapped energy in the CT exciting branch produces a unipolar decaying current with a fairly long time constant. This difference between primary and secondary currents is called a subsidence current (an example of a CT subsidence current is shown in Fig. 17) [17].

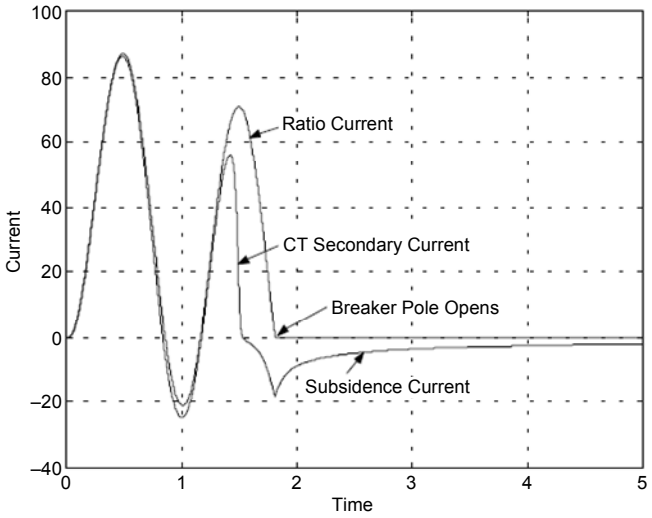

Fig. 17. Circuit breaker subsidence current.

The actual current peak in Fig. 16 is approximately 900 A primary current, the filtered current peak in Fig. 16 is approximately 580 A primary current, and the voltage spike in Fig. 14 is approximately 620 V. The relationship between the primary current flowing through the surge arrester and the secondary voltage appearing across the relay depends on the high-impedance bus differential relay secondary circuit, which is shown in Fig. 18.

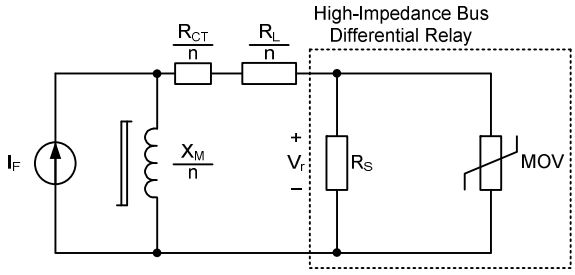

Fig. 18. High-impedance secondary circuit for internal bus fault.

The high-impedance bus protection at the 138 kV bus has five CT outputs paralleled to the relay, so *n* in Fig. 18 is equal to 5. R_{CT} is the resistance of the CT secondary winding, R_L is the lead resistance, X_M is the CT nonlinear excitation inductance, R_S is the 2000 Ω resistance of the high-impedance relay, and 87 is the differential element of the relay. In order to verify that the simulated current spike through the surge arrester and the voltage spike captured by the relay are representing the same event, the currents flowing in the secondary circuit at the moment of the 620 V voltage peak must be identified. Fig. 16 shows how the low-pass filtering decreases the current peak value; therefore, using 620 V across the CT secondary is a conservative estimate because the actual current peak might be considerably higher, as shown in Fig. 16.

The voltages across the CT excitation branch (X_M in Fig. 18) and the high-impedance relay (R_S in Fig. 18) are going to be approximately the same because the 2000 Ω resistor of the relay is much larger than R_{CT} and R_L. The total primary current flowing can be calculated using (4).

$$I_F = CTR \bullet (n \bullet I_e + I_r) \tag{4}$$

where:

CTR = 1200:5.

n = 5, the number of CTs at the bus.

I_e = the CT exciting current.

I_r = the relay current.

The CT exciting current depends on the CT accuracy class and the voltage across the CT. All five CTs are C800. Four of them are 1200:5 full ratio, but the capacitor bank CT is 2000:5 tapped down to 1200:5. The CT excitation characteristics (voltage versus current) for a typical C800 CT at full range are shown in Fig. 19.

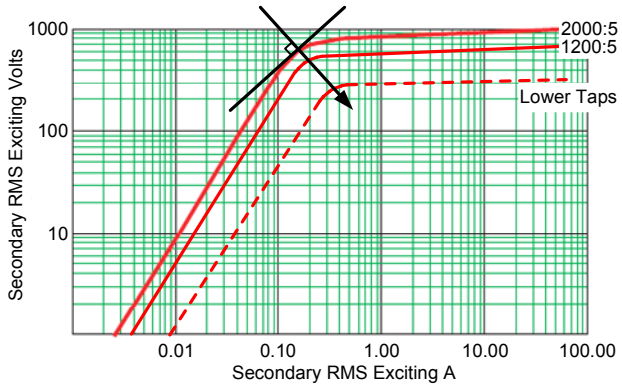

Fig. 19. CT nonlinear excitation characteristics.

From Fig. 14, we observe that the peak voltage (after the relay low-pass anti-aliasing filtering) is near 600 V. Fig. 19 shows that at 420 V_{rms} (600 V_{peak}), the secondary rms exciting current for the full range CT is approximately 0.14 A_{rms}. For the tapped down CT, the exciting current is approximately 1 A_{rms}. The peak relay current is calculated using (5).

$$I_r = \frac{V_r}{R_{2000}} = \frac{600}{2000} = 0.3 \text{ A} \tag{5}$$

When the CT exciting current (I_e) and the relay current (I_r) have been identified, the total primary peak current can be calculated using (6).

$$I_F = 240 \bullet \left[\left(4 \bullet 0.14 \bullet \sqrt{2}\right) + \left(1.0 \bullet \sqrt{2}\right) + \frac{600 \text{ V}}{2000\ \Omega} \right] \text{A} \tag{6}$$

$$I_F = 600 \text{ A}$$

The calculated fault current peak is very close to the 600 A simulated peak current. This verifies the theory that this relay misoperation was in fact due to a circuit breaker restrike.

VI. Settings Recommendations

Before any protection decisions are made, the relay passes the sampled waveform shown in Fig. 14 through a cosine filter to extract the 60 Hz frequency component from the sampled signal. The output of the cosine filter depends on the last 0.75 cycles of the sampled signal. The relay samples 16 times per power system cycle, so the 0.75-cycle cosine filter output depends on the last 12 samples (i.e., the last 0.75 cycles of data). Fig. 14 shows that the event only lasts for approximately 4 milliseconds, and the high-impedance relay samples approximately every millisecond for a 60 Hz power system. Fig. 14 also shows that the total length of the restrike event is less than 0.5 cycles. To prevent misoperation due to a circuit breaker restrike, a time delay must be added. The time delay needs to account for the event length, filter delay, and safety margin. Adding a 1.5-cycle time delay accounts for a 0.5-cycle event, 0.75-cycle filter delay, and 0.25-cycle safety margin. At least a 1.5-cycle time delay is recommended because it is difficult to predict the transient behavior of the power system, especially CT transient behavior, which greatly affects the signal measured by the relay. However, a time delay that is too long can decrease the dependability of the high-impedance bus protection, especially when lower-class CTs are used.

Note that increasing the instantaneous relay voltage setting can decrease, or even eliminate, the amount of time that the measured voltage exceeds the relay setting during a surge arrester operation. Reliable voltage settings should be determined for each application. Additionally, modern digital relays offer multiple differential elements, so one element may be enabled with a sensitive and time-delayed voltage setting while a second element may be enabled with a more secure and instantaneous voltage setting.

VII. Conclusion

Capacitor bank de-energization is highly demanding on the dielectric strength of the opening circuit breaker. The trapped charge remaining on the capacitor increases the voltage appearing across the circuit breaker, which increases the risk for circuit breaker restrikes. The transient overvoltage associated with circuit breaker restrikes can cause surge arresters located at the bus to start conducting current. The surge arrester current appears to the relay as differential current and can cause the relay to misoperate.

This paper reviews the concepts of capacitive switching, surge arresters, and high-impedance bus differential relays. This paper provides a detailed analysis of a real-world event caused by a circuit breaker restrike followed by a surge arrester conducting and a high-impedance bus differential relay misoperation. The real-world event was verified using EMTP simulations to prove that the misoperation was in fact due to a surge arrester conducting after a circuit breaker restrike.

When surge arresters are located within the zone of protection for a high-impedance bus differential relay, a time delay must be added to ensure secure relay operation.

VIII. Acknowledgment

The authors would like to thank Normann Fischer of Schweitzer Engineering Laboratories, Inc., for his help with performing some of the analysis in this paper.

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X. Biographies

Kristian (Kris) Koellner supervises the system protection department at the Lower Colorado River Authority (LCRA) in Austin, Texas. Prior to joining LCRA in 2010, Kris worked at Salt River Project (SRP) in Phoenix, Arizona, for sixteen years. Throughout his career, Kris has worked in the areas of distribution planning, power quality, and, most recently, system protection. Kris graduated with a B.S.E. degree in Electrical Engineering from Arizona State University and is registered as a professional engineer (PE) in the state of Texas. Kris served as the 2012 Chair of the ERCOT System Protection Working Group (SPWG).

Oskar Reynisson earned his bachelor's degree in electrical engineering from the University of Iceland in 2007 and worked for Rafteikning Consultant Engineers in Reykjavik, Iceland, for a year. He then began pursuing his master's degree with an emphasis in power systems at Michigan Technological University and graduated in 2011. Oskar joined Schweitzer Engineering Laboratories, Inc. in 2012 as an associate field application engineer. He is currently an IEEE member.

David Costello graduated from Texas A&M University in 1991 with a B.S.E.E. He worked as a system protection engineer at Central Power and Light and Central and Southwest Services in Texas and Oklahoma. He has served on the System Protection Task Force for ERCOT. In 1996, David joined Schweitzer Engineering Laboratories, Inc., where he has served as a field application engineer and regional service manager. He presently holds the title of technical support director and works in Fair Oaks Ranch, Texas. He is a senior member of IEEE, a member of the planning committee for the Conference for Protective Relay Engineers at Texas A&M University, and a recipient of the 2008 Walter A. Elmore Best Paper Award from the Georgia Institute of Technology Protective Relaying Conference.

Previously presented at the 2014 Texas A&M
Conference for Protective Relay Engineers.

20140210 • TP6599-01