Sizing Chokes for Mission-Critical Islanded Power Systems

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SIZING CHOKES FOR MISSION-CRITICAL ISLANDED POWER SYSTEMS

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Abstract—This paper shares a set of equations for sizing chokes for isolated-parallel power systems. The theory behind each equation is shared, and chokes are sized for an example power system.

Index Terms—Isolated-parallel, iso-parallel, IP bus, microgrid, resilience, offshore

I. INTRODUCTION

The reliability of islanded power systems can be improved by using isolated-parallel (IP) power system designs. IP methods are applicable for data centers, national security installations, offshore vessels, industrial processes, and hospitals. IP design methods improve power system resilience by providing fault tolerance, seamless islanding, faster generator synchronization, reduced voltage sensitivity to faults, and cost reductions for switchgear [1] [2]. This paper shares a set of boundary-value equations for selecting chokes in IP power systems.

IP systems typically use one IP choke per engine-generator (EG). Large groups of EGs, especially those operating at medium voltages, benefit from having smaller subgroups of EGs paralleled and the parallel buses connected to a common IP bus through IP chokes. A parallel bus containing multiple EGs is sometimes referred to as a standby power system. A typical IP configuration with multiple standby power systems is shown in Fig. 1.

Unlike IP systems arranged with EGs and chokes in a one-to-one ratio, the unit size of IP-connected parallel buses can change with the number of EGs connected at each parallel bus. Therefore, additional factors must be considered when selecting the reactive impedance and amperage capacity of the choke for this type of IP system. The method described in this paper is a first step in determining the appropriate size of an IP choke in a large IP system with paralleled EGs. Subsequent IP choke sizing methods require modeling and simulation, as described later in this paper.

II. CHOKE SIZING TO LIMIT CURRENT

Switchgear is rated for maximum allowable fault currents that must not be exceeded. The busbar bracing, structural strength, circuit breakers, current transformer sizes, and more are designed based on this current rating. Equation (1) (derived from Fig. 2) can be used to size a choke impedance (Z) so that it will not exceed this current rating.

$$Z > Z_R \left[\frac{N_{PAR}}{ISC_{MAX}(0.75)} - \frac{Z''_{PU}}{N_{EG}} \right] \quad (1)$$

where:

Z_R is the base impedance.

N_{PAR} is the total number of EG parallel buses.

ISC_{MAX} is the per-unit (pu) IP bus switchgear short-circuit rating.

Z''_{PU} is the EG subtransient reactance in pu.

N_{EG} is the number of EGs per parallel bus.

ISC_{MAX} is the maximum fault level the switchgear should experience. A value somewhat below the fault duty of the IP switchgear (e.g., 75 percent of the short-circuit bus brace rating) should be selected to account for X/R ratio asymmetry and possible fault contribution from connected loads. This explains the 0.75 value in (1).

In the following example there are three EGs on each parallel bus and the EG ratings are identical: 2,000 kW, 2,500 kVA, 10 kV, 60 Hz, and $Z''_{PU} = 0.1$. There are ten parallel buses on the IP bus, and the IP switchgear is rated at 25 kA.

First, the base current (I_R) and base impedance (Z_R) of the EG are calculated using (2) to complete the calculation of (1).

$$\begin{aligned} I_R &= \frac{kVAR}{\sqrt{3} \bullet V_R^{LL}} = \frac{2{,}500\ kVA}{\sqrt{3} \bullet 10\ kV} = 144.3\ A \\ Z_R &= \frac{V_R^{LL}}{\sqrt{3} \bullet I_R} = \frac{10{,}000}{\sqrt{3}} \bullet \frac{1}{144\ A} = 40\ \Omega \end{aligned} \quad (2)$$

where V_R is the base line-to-line (LL) voltage of the EG.

Then, the minimum impedance allowed per (1) is calculated using (3). The ohm value is divided by $2\pi \bullet 60$ to convert to milliHenrys (mH). The short-circuit rating of 25 kA is converted to pu by dividing by 144.3 A.

$$Z > Z_R \bullet \left(\frac{N_{PAR}}{\left(\frac{25{,}000\ A}{144.3\ A} \right) \bullet 0.75} - \frac{0.1}{3} \right) \bullet \frac{1}{2\pi \bullet 60} \quad (3)$$

$$Z > 4.63\ mH$$

Thus, the choke (a.k.a., reactor) must be larger than 4.63 mH to prevent switchgear damage.

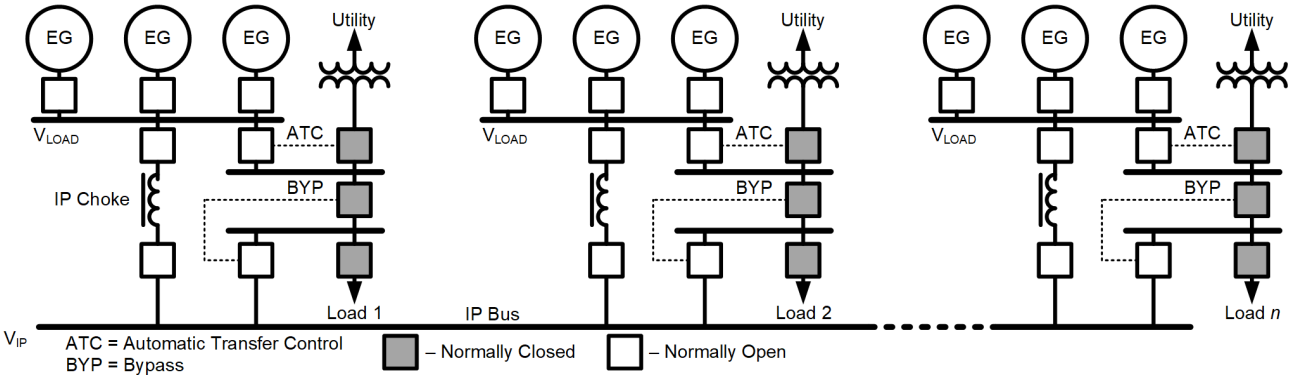

Fig. 1. Typical IP configuration

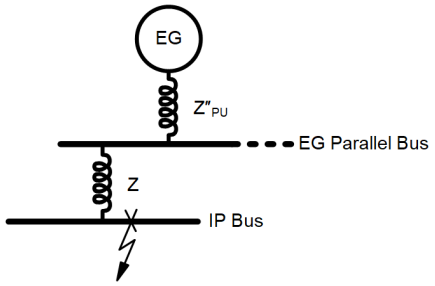

Fig. 2. Z limits fault current

III. CHOKE SIZING TO LIMIT VOLTAGE SAG

Choke impedances must be sized so as to keep processes online. Maintaining voltage during fault events keeps load contactors closed, variable speed drives online, and protective relays from tripping on low voltage. It is common to use curves such as the Computer and Business Equipment Manufacturers' Association (CBEMA) [3] or similar requirements to maintain an acceptable EG parallel bus voltage during an IP bus fault. A CBEMA type curve is shown in Fig. 3.

The examples in this section assume a system with fast, secure, and discriminating protective relays and fast circuit breakers. For example, a sag event down to 0.7 pu would be cleared by the relays and breakers in five cycles or less. The chokes should be sized to prevent the relays on breakers protecting the EGs from operating and de-energizing the power system.

For a fault on the IP bus, the ratio of the EG subtransient reactance (Z''_{PU}) and the choke impedance (Z) becomes an effective voltage divider. As the number of EGs on a parallel bus goes down, the Thévenin short-circuit impedance goes up (fewer machine impedances in parallel) and the parallel voltage goes down during a fault. The minimum parallel bus voltage during an IP bus fault occurs with one EG on the EG parallel bus. To confine the generator voltage dip to a certain percentage during an IP bus fault, Z must be selected according to (4).

$$Z > Z_R\left[\frac{Z''_{PU}}{N_{EG}} \bullet \frac{V_{MIN}}{1-V_{MIN}}\right] \tag{4}$$

V_{MIN} is the minimum EG parallel bus voltage (V_{LOAD}) allowed. This is commonly set based on the CBEMA Curve or on the minimum voltage requirements for low-voltage contactors, variable speed drives, and other critical loads. The single-line diagram to consider during this event is shown in Fig. 4.

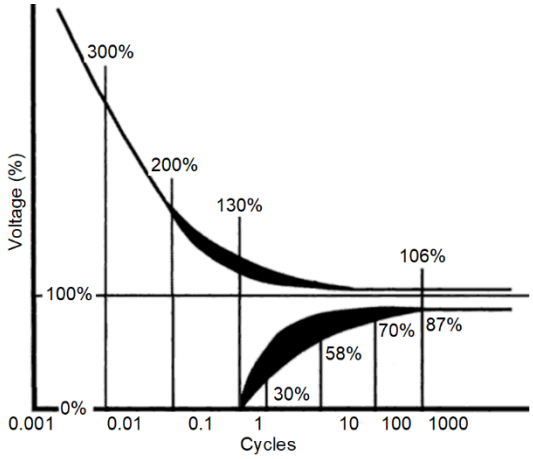

Fig. 3. Typical CBEMA Curve

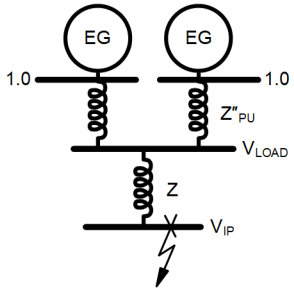

Fig. 4. Z limits voltage sag during faults

V_{IP} is the voltage on the IP bus, and V_{LOAD} is the voltage on the load bus.

Equation (5) assumes the ideal maximum voltage drop on the parallel buses for a fault on the IP bus of 30 percent (0.3 pu). $V_{MIN} = 0.7$ for the worst-case condition where $N_{EG} = 1$.

$$Z > \frac{40\ \text{mH}}{2\pi \bullet 60}\left[\frac{0.1}{1} \bullet \frac{0.7}{1-0.7}\right] \tag{5}$$
$$Z > 24.75\ \text{mH}$$

Thus, the reactor must be larger than 24.75 mH to prevent excessive voltage sag during a fault condition. If N_{EG} is held to a number greater than 1, the value of Z falls proportionally to $1/N_{EG}$.

IV. VAR CAPACITY LIMITATIONS

After determining the choke impedance required to manage voltage drop in a fault scenario, the steady-state volt-ampere reactive (VAR) requirements at the choke must be calculated. It is instructive to first review (6), the basic equation for power flow through a choke.

$$P = \frac{|V_{IN}| \bullet |V_{OUT}|}{Z} \sin\theta \quad (6)$$

Power flow (P) through a choke with an impedance (Z) creates a phase angle difference (θ) between voltage phasors at the choke's input (V_{IN}) and output (V_{OUT}). This is illustrated in Fig. 5.

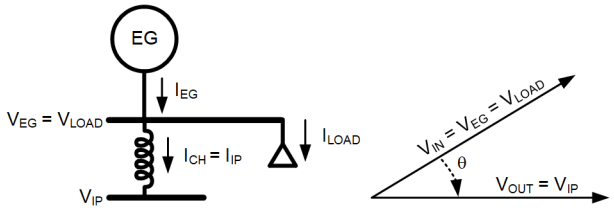

Fig. 5. Power transfer across the choke

I_{CH} is the current through the choke, which is equal to I_{IP}, the choke input current at the IP bus. I_{LOAD} is the load current, and I_{EG} is the cumulative EG current (the vector sum of I_{CH} and I_{LOAD}).

The EGs on an IP system are run non-isochronously (i.e., in a droop operation mode). Thus, the system frequency does not vary more than 0.6 Hz (for a 1 percent droop) so long as the engines are healthy and not overloaded. The value of Z (which is inversely proportional to frequency) does not change significantly as power flows (EG loading) change from zero to full load. Therefore, for this section Z is considered to be a constant. When V_{IN} is regulated by a healthy EG automatic voltage regulator (AVR) to 1.0 pu, an acceptable approximation of the power flow across a choke can be calculated by (7).

$$P\,pu = \frac{\sin\theta}{Z\,pu} \quad (7)$$

Equation (7) shows that the greater the impedance, the greater the angle between the input and output voltage phase angles for a given power flow.

As shown in Fig. 6, if the IP choke is assumed to have no resistance, then I_{CH} lags the voltage across the choke (V_{CH}) by exactly 90 degrees. V_{CH} is the phasor difference of V_{IP} and V_{LOAD} (the EG parallel bus voltage).

Both V_{IP} and V_{LOAD} are kept close to 1.0 pu by the AVRs' regulation of the EGs on both sides of the choke. Consequently, as shown in Fig. 6, V_{IP} and V_{LOAD} are equal in magnitude and the phase angle of I_{CH} lies midway between V_{IP} and V_{LOAD} on a phasor diagram.

The use of fewer directly connected motors and more variable speed drives allows the calculations to be simplified. Loads begin to approximate constant power unity power factor loads because variable speed drives and electronic power supplies consume very little out-of-phase current. Thus, I_{LOAD} is in phase with V_{LOAD}, as shown in Fig. 6. I_{LOAD} is the vector sum of I_{CH} and I_{EG}. This is true regardless of the directions of I_{CH} and V_{CH}, which depend on whether the IP choke is importing power into or exporting power out of the load bus. The magnitudes of I_{CH} and V_{CH}, and therefore the magnitude of angle θ, depend on the amount of power flowing through the choke, as calculated in (6).

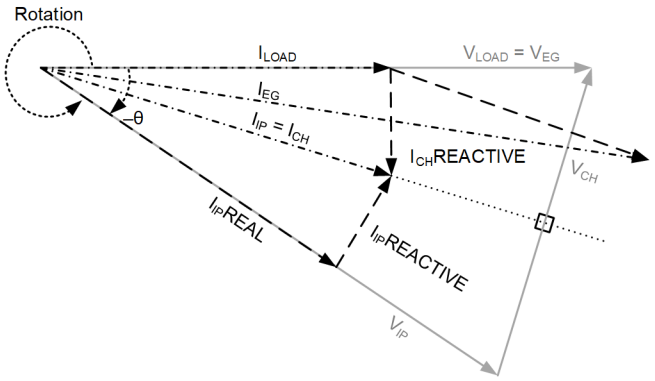

Fig. 6. IP phasor diagram

In this paper, the input of the IP choke is defined as the end connected to the IP bus and the output is defined as the end connected to the load bus. By this definition, when EG power exceeds load demand, as shown in Fig. 6, the power flow (P) through the IP choke is negative. The real portion of the choke's input current is in phase with V_{IP}, and the reactive portion of I_{IP} leads by 90 degrees. Because I_{IP} leads V_{IP} in the reactor, the choke appears capacitive from the IP bus and VARs flow into the choke from the IP bus (Q+) at the same time as watts flow out of the choke and into the IP bus (–P).

The real portion of the choke output current (I_{CH}) is in phase with the load voltage (V_{LOAD}) because the load in this situation is assumed to be unity power factor. The real portion of the EG current (I_{EG}), like the real portion of I_{CH}, is also in phase with V_{LOAD}. However, I_{EG} lags V_{LOAD} because the EGs (like the IP bus) supply positive VARs into the IP choke.

Fig. 6 shows that the reactive current elements of the IP choke at the choke input on the IP bus and the EG at the choke output on the load bus are equal and opposite. In other words, the VARs absorbed by the IP choke are supplied equally by the IP bus and the EGs, regardless of the phase angle (θ), which is determined by the amount of power flow through the choke.

In a situation where some of the EGs in parallel on the load bus are out of service, the IP choke's VAR demand may exceed the remaining EGs' capability curves. The load voltage will sag if the EG capabilities are exceeded. The combined VAR capacity of all EGs on the parallel bus must be greater than the total choke VAR load flowing into the choke to maintain 1.0 pu voltage on V_{LOAD}. Therefore, the VAR capacity of the EGs places a limit on how large the choke impedance (Z) can be to support a choke power flow (P) with a minimum number of EGs on the parallel bus.

The worst-case scenario occurs when a loaded parallel bus has the minimum number of EGs connected and the bypass breaker is open. For parallel buses with a combined load below 10 MW, this may be as few as one EG. (When no EGs are on the parallel bus, the load should be automatically bypassed to the IP bus.)

With only one EG on the bus, as shown in Fig. 7, the maximum choke impedance that can be supported without a drop in V_{LOAD} is determined as follows.

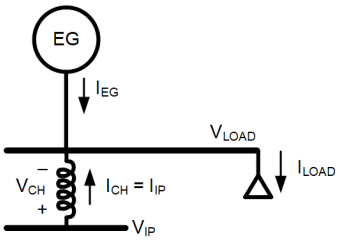

Fig. 7. Choke limits VAR flow under EG overload conditions

First, the P out of and the Q into the choke at the load bus are calculated using (8). The values of 0.6 and 0.8 come from a typical generator rated at 0.8 power factor (PF), as shown in Fig. 8.

$$\begin{aligned} P_{CHOKE} &= P_{LOAD} - N_{EG} \bullet kVA_{GEN}(0.8) \\ P_{CHOKE}{}^{PU} &= \frac{P_{CHOKE}}{P_B} \\ Q_{CHOKE} &= N_{EG} \bullet kVA_{GEN}(0.6) - Q_{LOAD} \end{aligned} \tag{8}$$

where:

P_{CHOKE} is the power transferred through the choke.

P_{LOAD} is the maximum real load that can be expected on the load bus.

kVA_{GEN} is the generator's three-phase nameplate kVA rating. If not published, assume the generator is rated at 0.8 PF and divide the generator kW by 0.8 to get kVA_{GEN}.

P_B is the base power (it is convenient to choose EGs rated in MVA).

Q_{CHOKE} is the reactive power transferred into the choke from the EG.

Q_{LOAD} is the maximum reactive load that can be expected on the load bus.

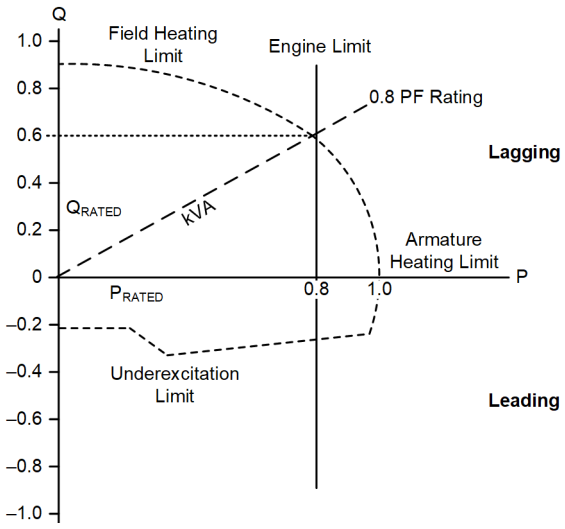

Fig. 8. Typical EG capability curve

Next, the load angle on the choke and the maximum choke impedance are calculated to prevent overloading of the EG, as shown in (9).

$$\begin{aligned} \alpha &= \tan^{-1}\left(\frac{Q_{CHOKE}}{P_{CHOKE}}\right) \\ Z &< Z_R \frac{1}{2\pi F}\left(\frac{\sin 2\alpha}{P_{CHOKE}{}^{PU}}\right) \end{aligned} \tag{9}$$

where α is the angle between I_{IP} and V_{IP} and is one-half of θ and F is the operating frequency.

Equation (10) shows how these equations are applied for a condition with one remaining EG rated at 2.5 MVA, 0.8 PF, and 6 MW of load at 1.0 PF.

$$\begin{aligned} P_{CHOKE} &= 6\text{ MW} - 1 \bullet 2.5\text{ MVA} \bullet 0.8 = 4\text{ MW} \\ P_B &= 2.5\text{ MVA} \\ P_{CHOKE}{}^{PU} &= \frac{4}{2.5} = 1.6\text{ pu Power} \\ Q_{CHOKE} &= -1 \bullet 2.5\text{ MVA} \bullet 0.6 + 0 = -1.5\text{ MVAR} \\ \alpha &= \tan^{-1}\left(\frac{1.5}{4}\right) = 20.55^\circ \\ Z &< \frac{40\ \Omega}{2\pi \bullet 60}\left(\frac{\sin(2 \bullet 20.55)}{1.6}\right) \\ Z &< 43.6\text{ mH} \end{aligned} \tag{10}$$

The largest allowable inductance to prevent AVR or generator overload is 43.6 mH.

V. DYNAMIC STABILITY CONSIDERATIONS

The stability of the standby power system is generally regarded as the ability of the EG to satisfy the following conditions:

1. Parallel EG buses stay in step. EG rotors can operate at different angles because of the large impedances between them.
2. System frequency is within a few hertz.
3. Voltages do not collapse due to AVR overload, exciter current limits being exceeded, or generator saturation.
4. Conditions such as V/Hz, undervoltage, overvoltage, underfrequency, and overfrequency are avoided to prevent protective relay actions.

These stability problems must be modeled and confirmed prior to final choke selection. The authors advise the use of real-time, hardware-in-the-loop (HIL) modeling prior to choke selection. This technique allows protective relays and microgrid controllers to be connected in a closed loop with the simulated environment. It is advisable to perform HIL testing prior to finalizing an IP power system design. This technique has proven advantageous in many industries [4] [5].

Keeping generators in step is of concern for large chokes and large power flow conditions. For example, load steps on one parallel bus will cause load swings among other parallel EG buses. The IP bus must be able to quickly pass current from machine to machine to keep parallel buses in step, effectively transferring inertial energy back and forth. High-impedance IP chokes can inhibit the required current flow. This most often

manifests as VAR flow restrictions and can result in excessive oscillatory swinging or even out-of-step behavior.

Two control settings that can improve stability are governor power droop (Hz/kW) and AVR reactive power droop (V/kVAR). Governor and AVR droop improve stability under high impedances and large load swings. Engine governors and AVR field excitation control systems must be selected very carefully to avoid unnecessary overloads, swinging, out-of-step behavior, or worse. When a high IP choke impedance is necessary, system stability may rely on EG governor and AVR control methods. In addition to improving transient stability, both governor and AVR droop are required for load sharing between EGs on an IP system. Isochronous speed load sharing controls do not work.

The prevalence of variable speed drives and electronic loads (as opposed to the historical use of directly connected motor loads) means that the electric power consumed is determined by the motor process loads and not the power system. These loads do not change their power usage as frequency and voltage change, unlike directly connected motors, which do exhibit sensitivity to voltage and frequency. This means that modern loads exhibit negative impedance (i.e., they draw more current as voltage drops to ensure a constant power demand). Such loads tend to make the use of AVR droop less effective.

Modeling of IP standby systems with control HIL (cHIL) digital simulation methods is highly recommended to establish governor and AVR settings prior to purchasing equipment. This saves time and can prevent damage to system elements. To make a simulation accurate, the programmer must know all the electrical characteristics of the EGs, chokes, and switchgear as well as the rotational inertia values of the machinery and control transfer function values for the engine governor and AVRs. Because many EG manufacturers will not share their control loops, a more reliable way to ensure an accurate cHIL model is to perform load acceptance and rejection tests on a live machine. The data from these tests can then be used to build a model that matches field performance.

Accurate cHIL models can identify unstable operational conditions. Fig. 9 shows a digital simulation performed on an IP standby system. The voltage, current, and differential phase angle traces show a load step at 3 seconds causing a parallel bus to break out-of-step within 1 second. Significant voltage deviations and excessively high currents are displayed.

After making incremental increases in the speed and voltage droop settings, the load step then produced the traces shown in Fig. 10.

Oscillations in frequency and circulating current are expected in rotating systems with large amounts of inertia and high impedances. However, the ultimate goal of the standby power system is to provide smooth, continuous voltage to the load. A real-time HIL simulation environment is the best tool to ensure that this is accomplished.

VI. OTHER RATING CONSIDERATIONS

An allowance of approximately 5 percent overvoltage should be made in selecting chokes to account for dc offsets associated with X/R ratios. For example, the choke voltage rating should be 6 kV for an IP bus rated at 5,773 V.

The IP choke amperage rating should be at least 125 percent of the full-load current, assuming all EGs on the bus are out of service. They should also be rated at 150 percent for 10 seconds.

VII. CONCLUSIONS

The calculations in this paper produce a range of choke values suitable for pricing specifications and planning purposes. In the example, the workable values of the IP choke range from roughly 25 to 43 mH, provided the load does not exhibit significant VAR demand and that a momentary 30 percent voltage drop is acceptable. To accommodate load VARs, a value at the low end of the range is desirable and may also be less costly.

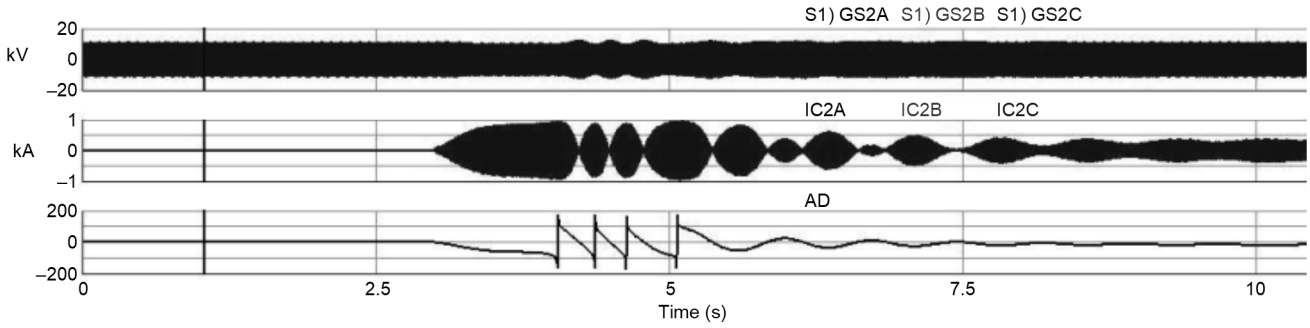

Fig. 9. Rotor angle instability without droop

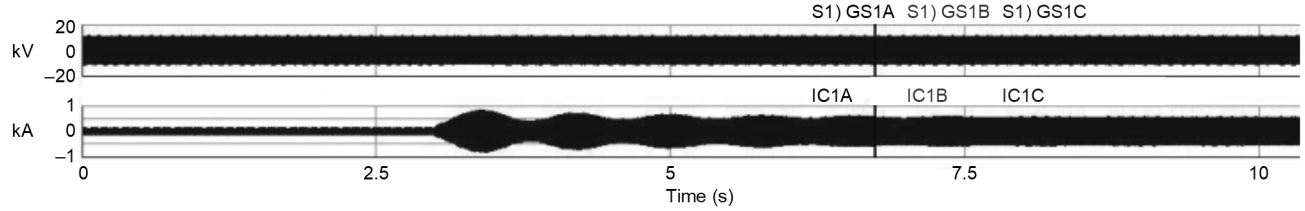

Fig. 10. Rotor angle instability fixed by droop

Both governor and AVR droop are required for load sharing between EGs on an IP system. Isochronous speed load sharing controls do not work for this application.

Real-time simulation of the IP standby power system should be run to verify performance stability and to confirm the choke sizing, governor controls, and AVR controls. This method allows an engineer to test the governor and AVR controls to find the right compromise between fault current limiting and operational stability.

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IX. VITAE

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